UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/976,731	10/12/2001	Leilei Song	3	2455

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Ryan, Mason & Lewis, LLP
Suite 205
1300 Post Road
Fairfield, CT 06430

EXAMINER
TORRES, JOSEPH D

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 07/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)
Office Action Summary	09/976,731	SONG, LEILEI
	Examiner	Art Unit
	Joseph D. Torres	2133

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>15 May 2006</u>.

2a)☒ This action is **FINAL**.   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>1-10,25 and 26</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>1-4,7-10,25 and 26</u> is/are rejected.

7)☒ Claim(s) <u>5 and 6</u> is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on <u>26 April 2004</u> is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

       1.☐ Certified copies of the priority documents have been received.

       2.☐ Certified copies of the priority documents have been received in Application No. _____.

       3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the·International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

Response to Arguments

1.   Applicant's arguments filed 05/15/2006 have been fully considered but they are

not persuasive.

The Applicant contends, "Regarding the written description requirement, the Examiner

asserts that "nowhere in the specification does the Applicant teach 'wherein said

reduced power mode consumes less power in a given interval of time relative to a

normal operating mode' and in particular, the Applicant never mentions 'operating

mode' much less 'normal operating mode' anywhere in the specification."

    Applicant notes that the present disclosure teaches that the reduced

power mode consumes less power relative to a normal operating mode: on, for

example, page 2; lines 9-28, and page 13, line 13, to page 17, line 11. A person of

ordinary skill in the art would recognize that power is measured per unit of time. For

example, a "watt" is defined as "an International System unit of power equal to one joule

per second." (See, dictionary.com; emphasis added.)

    Thus, a person of ordinary skill in the art would understand that one mode can

"consume less power in a given interval of time" than another mode. Applicant also

notes that, in the context of the present invention, a person of ordinary skill in the art

would recognize the meaning of the terms "operating mode" and "normal operating

mode." Thus, in light of the present specification, a person of ordinary skill in the art

would understand the meaning of the phrase "wherein said reduced power mode

consumes less power in a given interval of time relative to a normal operating mode.""

The Examiner asserts that one of ordinary skill in the art at the time the invention was

made would not find where the Applicant teaches `wherein said reduced power mode

consumes less power in a given interval of time relative to a normal operating mode' in

any part of the Applicant's specification. There is nothing in the Application that teaches

what a normal operating mode is and how it distinguishes itself from the multitude of

other modes taught in the Applicant's specification such as "low power mode" in lines

12-13 on page 14; "Opcode 3" mode in line 19 on page 14; "Opcode 0" mode in line 3

on page 15; or any of the following four modes in lines 1-5 on page 25 of the Applicant's

disclosure: (1) decoder enable (i.e., decode and carry out error correction); (2)

monitoring mode (i.e., decode, calculate error information without error correction); (3)

decoder disabled and output incoming data after decoder-latency delay mode; and (4)

decoder disabled and output incoming data without delay mode.

The Examiner asserts that the language "wherein said reduced power mode consumes

less power in a given interval of time relative to a normal operating mode" was

introduced in the amendment filed 12/22/2005 without any regard to what is taught in

the Applicant's specification for the sole purpose of introducing new language to

overcome Prior Art rejections. In the Applicant's current response the Applicant now

suggests that support for the amended language can be found somewhere in page 2;

lines 9-28, and page 13, line 13, to page 17, line 11, but does not say what the support

is nor does the Applicant show how any language in the cited pages provides support

for the language.

The Applicant contends, "Contrary to the Examiner's assertion, the cited claims are

definite since they specifically recite the two modes (reduced power mode and normal

operating mode) and recite how the reduced power mode compares to a normal

operating mode, i.e., the reduced power mode consumes less power in a given interval

of time relative to (than) a normal operating mode".

The Examiner disagrees and asserts that there is nothing in the specification or the

claim to even distinguish "reduced power mode" from "normal operating mode". There

is nothing in the Application that teaches what a normal operating mode is and how it

distinguishes itself from the multitude of other modes taught in the Applicant's

specification such as "low power mode" in lines 12-13 on page 14; "Opcode 3" mode in

line 19 on page 14; "Opcode 0" mode in line 3 on page 15; or any of the following four

modes in lines 1-5 on page 25 of the Applicant's disclosure: (1) decoder enable (i.e.,

decode and carry out error correction); (2) monitoring mode (i.e., decode, calculate error

information without error correction); (3) decoder disabled and output incoming data

after decoder-latency delay mode; and (4) decoder disabled and output incoming data

without delay mode. The amended language filed 12/22/2005 is contrived for the sole

purpose of overcoming Prior Art rejections without any regard to what is taught in the

Applicant's specification.

The Applicant contends, "Regarding the Examiner's rejection of the cited claims as

being incomplete for omitting essential steps, such omission amounting to a gap

between the steps, the Examiner asserts that the omitted elements are: the relationship

between "given interval of time" and "normal operating mode;" and the relationship

between "reduced power mode" and "given interval of time."

Applicant notes that the relationships between operational modes (e.g., a

normal operating mode and a reduced power mode) and an interval of time are inherent

relationships, i.e., each mode inherently operates over an interval of tine, and inherently

consumes a certain amount of power per unit of time, as would be apparent to a person

of ordinary skill in the art".

If the Applicant believes the language is inherent then the language should be removed

form the claim since it fails to add a meaningful limitation.

The Applicant contends, "Applicant notes that, as the Examiner acknowledges, Noguchi

teaches that error correction is terminated to reduce power consumption (see, cot. 3,

lines 12-25; cot. 5, lines 54-62; cot. 9, lines 18-40 and 54-60). Noguchi teaches, for

example, that,

> further, the clock signal which is supplied to the data error correction
> device is stopped during a period after the error correction processing is
> terminated when the decoding has been repeated less than the predetermined
> number of times,.till the iterative decoding for the next data is started. Therefore,
> the power consumption in the data error correction device can be further
> reduced. (Col. 9, lines 54-60; emphasis added.)

Noguchi teaches to terminate error correction and, as a result, reduces power

consumption; the present disclosure teaches to perform error correction in a reduced

power mode. The specific language of cot. 9, lines 54-60, controls over the general

language cited by the Examiner at cot. 4, lines 61-67. Thus, a person of ordinary skill in

the art would understand

Noguchi as teaching to terminate error correction to reduce power consumption.

The present disclosure teaches to perform error correction in a reduced power mode.

Independent claims 1, 25, and 16 require that the reduced power mode consumes less

power in a given interval of time relative to a normal operating mode. Support for this

amendment can be found on page 2, lines 15-18; page 13, lines 13-17; page 14, lines

12-18; page 15, lines 23-27; and page 21, lines 17-30, of the originally filed

specification".

Noguchi teaches exactly what Noguchi says in the recited excerpt "**the clock signal**

which is supplied to the data error correction device **is stopped** during a period after the

error correction **processing** is terminated to reduce power consumption". Noguchi

teaches that the **clock signal is stopped** during a period after the error correction

processing is terminated. Furthermore; in the same excerpt, Noguchi explicitly

teaches that the clock remains stopped until the iterative decoding for the next data is

started. Col. 3, lines 16-20 in Noguchi explicitly teaches "correct termination judgement

means 34 judges that all errors in the data are corrected, and outputs the judgement

result that the correction is to be terminated to the control means 35. The control means

35 controls the syndrome calculation means 31 and the like, **to execute the iterative**

decoding for data which are to be subjected to the error correction processing

next, without interruption" [Emphasis Added]. That is, error correction processing of

a current codeword is stopped and error correction processing of the next codeword
begins without interruption. The Examiner asserts the error correction processing of the
next codeword cannot take place if the error correction device is turned off. Noguchi
teaches in the Noguchi patent exactly what the Abstract in Noguchi states, "the number
of times of the iterative decoding can be reduced with ensuring the reliability of data as
in the case where the data are corrected the maximum number of times, thereby
realizing the reduced power consumption in the error correction processing". That is,
Noguchi teaches reducing power consumption in an iterative error correction decoder
by reducing the number of iterations in the iterative error correction decoder from a
maximum number of iterations that would normally take place, if the power reduction
algorithm in Noguchi were not implemented, while operating the iterative error
correction decoder, without interruption, so that the iterative error correction decoder
can continually correct a next codeword immediately after terminating error correction
for a current codeword.

The Applicant contends, "Noguchi and Cameron, alone or in combination, do not
disclose or suggest providing a plurality of intermediate polynomials, and wherein the
step of reducing power consumption in the error correction system when the actual
number of errors is less than the maximum error correction capability further comprises
the step of determining if a degree of at least one of the intermediate polynomials is less
than a predetermined degree, as required by claim 3".

The Examiner disagrees and asserts that the Abstract in Cameron teaches that the test

for uncorrectable errors comprises determining if the degree of the Error Locator

Polynomial $\Lambda(x)$ and the degree of the Error Magnitude Polynomial $\Omega(x)$ are less than

predetermined values. One of ordinary skill in the art at the time the invention was

made would have known that the Error Locator Polynomial $\Lambda(x)$ and the degree of the

Error Magnitude Polynomial $\Omega(x)$ are intermediate polynomials and uncorrectable errors

are a result of exceeding the maximum error correction capability of a code.

The Applicant contends that Noguchi and Cameron, alone or in combination, do not

disclose or suggest "wherein one intermediate polynomial is a first error evaluator

polynomial R(x), wherein one intermediate polynomial is a first error locator polynomial

F(x), wherein $R^{(r+1)}(x) = F^{(r+1)}(x) \cdot S(x) \bmod x^{2t}$ wherein r is a number of iterations, S(x) is

a syndrome polynomial, and t is a number of errors capable of being corrected, wherein

one intermediate polynomial is a second error evaluator polynomial Q(x), wherein one

intermediate polynomial is a second error locator polynomial G(x), wherein $Q^{(r+1)}(x) =$

$G^{(r+1)}(x) \cdot S(x) \bmod x^{2t}$, wherein the step of determining if a degree of at least one of the

intermediate polynomials is less than a predetermined degree further comprises the

step of determining if a degree of either R(x) or Q(x) is less than a predetermined

degree, wherein R(x) and F(x) are valid when a degree of R(x) is less than the

predetermined degree, and wherein Q(x) and G(x) are valid when a degree of Q(x) is

less than the predetermined degree, as required by claim 4".

The Examiner disagrees and asserts that even the Applicant acknowledges on page 11

of the Applicant's disclosure that the equations in claim 4 are equations specified by the

Modified Euclidean Algorithm. The Modified Euclidean Algorithm is not the Applicant's

invention just as the equations of claim 4 are not the Applicant's invention.

The Applicant contends, "Noguchi and Cameron, alone or in combination, do not

disclose or suggest determining a plurality of syndromes; determining if all of the

syndromes have a predetermined value; and reducing power consumption of the

decoder of the error correction system when all of the syndromes have the

predetermined value, as required by claim 7".

The Examiner disagrees and asserts that Figure 2 in Noguchi teaches that whenever

SYN(B1)=0 and UNC(A1)=0, correction is terminated thereby reducing power. Note:

one of ordinary skill in the art at the time the invention was made that SYN(B1) can only

equal zero when all of the syndromes of the codeword B1 equal the predetermined

value of zero.

Claim Rejections - 35 USC § 112 (as copied from the Previous Office Action)

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2.   Claims 1-10, 25 and 26 are rejected under 35 U.S.C. 112, first paragraph, as

failing to comply with the written description requirement. The claim(s) contains subject

matter which was not described in the specification in such a way as to reasonably

convey to one skilled in the relevant art that the inventor(s), at the time the application

was filed, had possession of the claimed invention. Claims 1, 25 and 26 recite "wherein

said reduced power mode consumes less power in a given interval of time relative to a

normal operating mode". Nowhere in the specification does the Applicant teach

"wherein said reduced power mode consumes less power in a given interval of time

relative to a normal operating mode" and in particular, the Applicant never mentions

"operating mode" much less "normal operating mode" anywhere in the specification.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly
claiming the subject matter which the applicant regards as his invention.

3.   Claims 1-10, 25 and 26 are rejected under 35 U.S.C. 112, second paragraph, as

being indefinite for failing to particularly point out and distinctly claim the subject matter

which applicant regards as the invention.

Claims 1, 25 and 26 recite "wherein said reduced power mode consumes less power in

a given interval of time relative to a normal operating mode".

The term "relative to" in is a relative term which renders the claims indefinite. The term

"relative to" is not defined by the claim, the specification does not provide a standard for

ascertaining the requisite degree, and one of ordinary skill in the art would not be

reasonably apprised of the scope of the invention.

Claims 1, 25 and 26 are rejected under 35 U.S.C. 112, second paragraph, as being

incomplete for omitting essential elements, such omission amounting to a gap between

the elements. See MPEP § 2172.01. Claims 1, 25 and 26 recite "wherein said reduced

power mode consumes less power in a given interval of time relative to a normal

operating mode". The omitted elements are: the relationship between "given interval of

time" and "normal operating mode". The omitted elements are: the relationship between

"reduced power mode" and "given interval of time".

Claim Rejections - 35 USC § 102 (as copied from the Previous Office Action)

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by
another filed in the United States before the invention by the applicant for patent or (2) a patent
granted on an application for patent by another filed in the United States before the invention by the
applicant for patent, except that an international application filed under the treaty defined in section
351(a) shall have the effects for purposes of this subsection of an application filed in the United States
only if the international application designated the United States and was published under Article 21(2)
of such treaty in the English language.

4.   Claims 1, 2, 7, 8, 25 and 26 are rejected under 35 U.S.C. 102(e) as being

anticiapted by Noguchi; Nobuaki (US 6611939 B1).

35 U.S.C. 102(e) rejection of claims 1, 25 and 26.

Noguchi teaches determining if an actual number of errors is less than a maximum error

correction capability (Figure 2 in Noguchi teaches determining if uncorrectable errors

exist and flagging the uncorrectable errors with flags, UNC(A1), UNC(B1), UNC(A2) &

UNC(B2), i.e., if UNC(A1)=0 there are no uncorrectable errors with respect to the A1

decoding and the actual numbers are below the maximum error correction capability of

the A1 decoding, if UNC(B1)=0 there are no uncorrectable errors with respect to the B1

decoding and the actual numbers are below the maximum error correction capability of

the B1 decoding, if UNC(A2)=0 there are no uncorrectable errors with respect to the A2

decoding and the actual numbers are below the maximum error correction capability of

the A2 decoding & if UNC(B2)=0 there are no uncorrectable errors with respect to the

B2 decoding and the actual numbers are below the maximum error correction capability

of the B2 decoding); and performing error correction in a reduced power mode in a

decoder of the error correction system when the actual number of errors is less than the

maximum error correction capability (Step S3 in Figure 2 of Noguchi teaches that when

UNC(A1)=0, i.e., the actual numbers are below the maximum error correction capability

of the A1 decoding correction is terminated; Note: the abstract in Noguchi teaches that

error correction is terminated to reduce power consumption; hence Noguchi teaches

performing error correction in a reduced power mode in a decoder of the error

correction system when the actual number of errors is less than the maximum error

correction capability, that is; when UNC(A1)=0; **Note also that Figure 2 in Noguchi is**

an error correction algorithm for an error correction process and that the

termination routine taught in Noguchi is incorporated into the error correction

process as a part of the error correction process that is the error correction

process taught in Noguchi *is* a reduced power error correction process whereby

error correction is explicitly performed in a reduced power mode in the decoder

of the error correction-system used for implementing the reduced power error

correction process taught in Noguchi when the actual number of errors is less

than the maximum error correction capability), wherein said reduced power mode

consumes less power in a given interval of time relative to a normal operating mode

(Figure 1 in Noguchi is a data correction device capable of terminating operations to

conserve power when error correction is not needed, Data Error Correction Device 20

receives input data codewords to determine error locations and error values of

erroneous data codewords that are provided to a data processing device for the

purposes of correcting and decoding erroneous data codewords and does not

implement any type of error correction or decoding of data codewords itself; that is,

nowhere does Noguchi teach any output from the Data Error Correction Device 20 that

would alter the timing or clocking of any other device so one can only assume that

codewords are processed and decoded in another device separate from the Data Error

Correction Device 20 without altering the normal timing of the decoding process in any

other device necessary for error correction; Noguchi only teaches a means for saving

power in on component, the Data Error Correction Device 20 in Figure 1 of Noguchi,

and does not teach anywhere in the Noguchi patent the alteration of normal timing in

any other device associated with error correction).

35 U.S.C. 102(e) rejection of claim 2.

See col. 10, lines 36-44 in Noguchi. Note: The Authoritative Dictionary of IEEE

Standards Terms defines gating as the application of inhibiting pulses during part of a

cycle of equipment operation; hence stopping a clock as taught in col. 10, lines 36-44 of

Noguchi is a means for gating.

35 U.S.C. 102(e) rejection of claims 7 and 8.

Col. 7, lines 1-5 in Noguchi teaches that SYN(A1), SYN(B1), SYN(A2) & SYN(B2) are

flags and are set to 0 if all the syndromes for the respective decodings are zero.

Syndrome calculation means 11 in Figure 1 of Noguchi is a means for determining a

number of syndromes. Flagging the B1 decoding using the SYN(B1) flag is a means for

determining if all the syndromes have the predetermined value of zero or not. Figure 2

in Noguchi teaches that whenever SYN(B1)=0 and UNC(A1)=0, correction is terminated

thereby reducing power. **Note: one of ordinary skill in the art at the time the**

invention was made that SYN(B1) can only equal zero when all of the syndromes

of the codeword B1 equal the predetermined value of zero.

Claim Rejections - 35 USC § 103 (as copied from the Previous Office Action)

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148

USPQ 459 (1966), that are applied for establishing a background for determining

obviousness under 35 U.S.C. 103(a) are summarized as follows:

      1.   Determining the scope and contents of the prior art.

      2.   Ascertaining the differences between the prior art and the claims at issue.

      3.   Resolving the level of ordinary skill in the pertinent art.

      4.   Considering objective evidence present in the application indicating obviousness or nonobviousness.

5.   Claims 3, 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Noguchi; Nobuaki (US 6611939 B1) in view of Cameron; Kelly (US 5099482 A).

35 U.S.C. 103(a) rejection of claims 3 and 9.

Noguchi substantially teaches the claimed invention described in claims 1, 2, 7 and 8 (as rejected above).

However Noguchi does not explicitly teach the specific use of the particular elements of a decoder for Reed-Solomon codes nor does Noguchi teach how an uncorrectable error is determined.

Cameron, in an analogous art, teaches use of the particular elements of a decoder for Reed-Solomon codes and how an uncorrectable error is determined from intermediate polynomials (Note: the Abstract in Cameron teaches that the test for uncorrectable errors comprises determining if the degree of the Error Locator Polynomial $4(x)$ and the degree of the Error Magnitude Polynomial $A(x)$ are less than predetermined values).

Note: Noguchi teaches general syndrome based error correction codes, which include Reed-Solomon codes whereas Cameron explicitly focuses on a specific type of syndrome based code, i.e., Reed-Solomon codes. Note: one of ordinary skill in the art at the time the invention was made would have been highly motivated to use a Reed-

Solomon code since Reed-Solomon codes form the core of the most powerful known algebraic codes.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Noguchi with the teachings of Cameron by including use of the particular elements of a decoder for Reed-Solomon codes. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of the particular elements of a decoder for Reed-Solomon codes would have provided the opportunity for using one of the most powerful known algebraic codes.

35 U.S.C. 103(a) rejection of claim 10.

If the Syndromes are not all zero, error correction circuitry is enabled to correct errors. Calculating error polynomials is a required step for decoding Reed-Solomon codes.

6.   Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Noguchi; Nobuaki (US 6611939 B1) and Cameron; Kelly (US 5099482 A) in view of Oh; Kyu-taeg et al. (US 6256763 B1, hereafter referred to as Oh).

35 U.S.C. 103(a) rejection of claim 4.

Noguchi and Cameron substantially teaches the claimed invention described in claims 1-3 (as rejected above).

However Noguchi and Cameron do not explicitly teach the specific use of the modified

Euclidean Algorithm.

Oh, in an analogous art, teaches use of the modified Euclidean Algorithm (Figure 1 in

Oh).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the

invention was made to modify Noguchi and Cameron with the teachings of Oh by

including use of the modified Euclidean Algorithm. This modification would have been

obvious to one of ordinary skill in the art, at the time the invention was made, because

one of ordinary skill in the art would have recognized that use of the modified Euclidean

Algorithm would have provided power consumption reduction and complexity reduction

aspects.

Allowable Subject Matter (as copied from the Previous Office Action)

7.   Claims 5 and 6 are objected to as being dependent upon a rejected base claim,

but would be allowable if rewritten in independent form including all of the limitations of

the base claim and any intervening claims.

Conclusion

8.   **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time

policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within
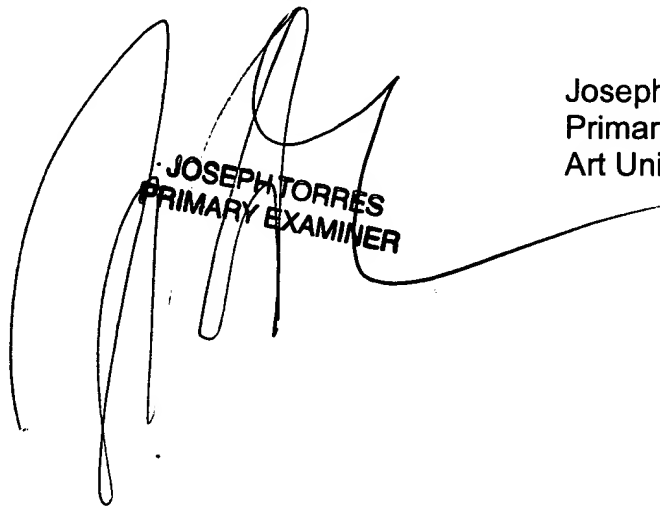
TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (571) 272-3829. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published

applications may be obtained from either Private PAIR or Public PAIR. Status

information for unpublished applications is available through Private PAIR only. For

more information about the PAIR system, see http://pair-direct.uspto.gov. Should you

have questions on access to the Private PAIR system, contact the Electronic Business

Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO

Customer Service Representative or access to the automated information system, call

800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Joseph D. Torres, PhD
Primary Examiner
Art Unit 2133